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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/560,397	04/11/2006	Takefumi Nishimuta	5000-5295	2526

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EXAMINER	
PATTON, PAUL E	
ART UNIT	**PAPER NUMBER**
2822	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/560,397	NISHIMUTA ET AL.	
	Examiner	Art Unit	
	Paul E. Patton	2809	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/11/2006*

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *4/11/2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/12/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1- 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hieda (JP 2001-224740) Hieda, in view of Ohmi (USPAT 6975018 B2) Ohmi and further in view of Mitsuru (JP 09-323292) Mitsuru.

3. As to claims 1 and 6, Hieda discloses and shows (Fig 1) a MIS Field-effect transistor in which a projecting portion (17) is formed by a silicon substrate (10) having a first crystal surface (13) as a primary surface and a second crystal surface (17) as a side surface, a gate insulating film (18) is formed on at least part of the top surface and the side surface of the projecting portion, a gate (16) is formed on the gate insulating film, and a drain and a source (22) are formed on both sides enclosing the gate insulating film of the projecting portion.

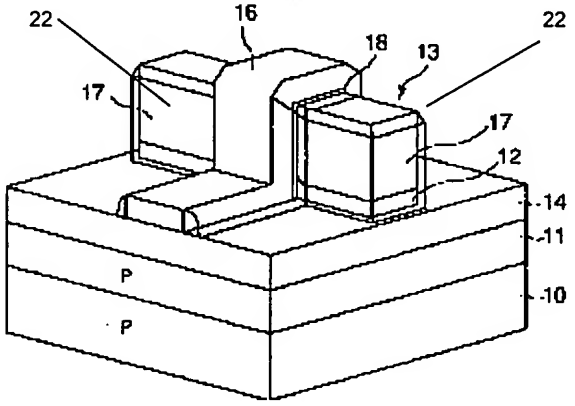

Fig 1

4. Hieda does not disclose that terminated hydrogen on the silicon surface is removed in a plasma atmosphere on an inert gas, nor does he state that the gate insulating film is formed at a temperature at or lower than about 550°C in the plasma atmosphere.

5. Ohmi discloses that terminated hydrogen on the silicon surface is removed in a plasma atmosphere on an inert gas (Column 3, lines 50-53), and states that the gate insulating film is formed at a temperature at or lower than about 550°C in the plasma atmosphere (Column 4, lines 26-32)

6. Ohmi is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to use plasma and inert gas to remove terminated hydrogen and to form a gate insulating film at temperatures at or lower than about 550°C.

7. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hieda by using plasma and inert gas to remove terminated hydrogen and to form a gate insulating film at temperatures at or lower than about 550°C to obtain advantages such as maintaining uniformity of film formation across large substrates and reduced leakage current according to the teachings of Ohmi (Column 1,lines 42-48 and Column 2, lines 1-10).

8. Hieda as modified by Ohmi does not disclose that the claimed circuit includes a capacitor and a p-channel MIS field-effect transistor or an n-channel MIS field-effect transistor.

9. Mitsuru shows (Mitsuru, Fig 2) a switched capacitor circuit (101) including a capacitor (4) and a p-channel MIS field-effect transistor or an n-channel MIS field-effect transistor.

10. Mitsuru is evidence that a switched capacitor circuit requires a capacitor and at least a field-effect transistor to complete the formation.

11. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hieda as modified by Ohmi to include a capacitor and at least a field-effect transistor in order to complete the switched capacitor circuit according to the teachings of Mitsuru.

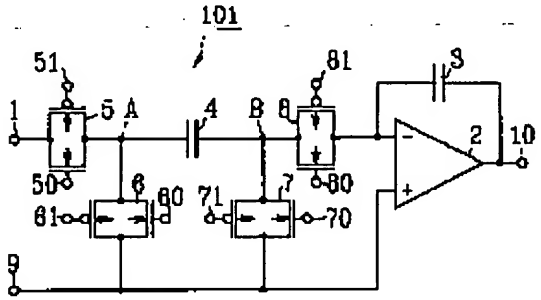

Fig 2

12. As to claim 2, Hieda discloses and shows (Fig 1) that a channel (22) is formed on a first crystal surface of a top surface (13) and a second crystal surface (17) of the projecting portion and the channel width of the MIS field-effect transistor is a total of a channel width of the top surface and a channel width of the side surface (Hieda, paragraph [0016]).

13. As to claim 3, Hieda discloses and shows (Fig 1 and 2) the projecting portion has a top surface comprising a silicon surface (100) (Paragraph [0036]), and the source (S) and drain (D) are formed on the projecting portion enclosing the gate and in left and right area of the projecting portion of the silicon substrate (Fig 3).

14. Hieda does not explicitly disclose that the side surface of the projecting portion has a crystal orientation of (110). Given the well-known nature of crystalline silicon the orientation of the side surface as (110) would have at least been obvious.

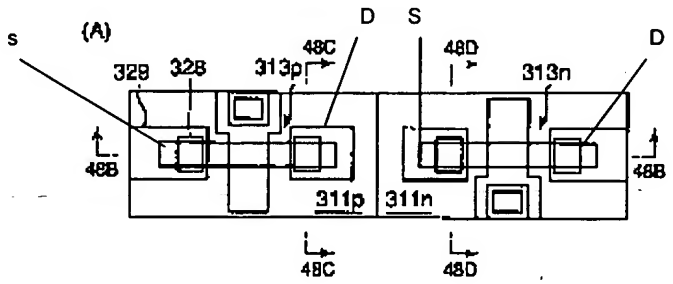

Fig 3

15. As to claims 4, 7 and 8, Hieda discloses that the gate width of a top surface and the side surface of the projecting portion of the p-channel MIS field-effect transistor is set such that current drive capability of the p-channel MIS field-effect transistor can be substantially equal to current drive capability of the n-channel MIS field-effect transistor (Paragraphs [0259 and [0260]).

16. Hieda as modified by Ohmi does not disclose a switched capacitor circuit comprising a switch formed by connecting in parallel a p-channel MIS field-effect transistor and n-channel field-effect transistor

17. Mitsuru shows (Mitsuru, Fig 2) a switched capacitor circuit comprising a switch formed by connecting in parallel a p-channel MIS field-effect transistor and n-channel field-effect transistor.

18. Mitsuru is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to use a switched capacitor circuit comprising a switch formed

by connecting in parallel a p-channel MIS field-effect transistor and n-channel field-effect transistor.

19. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hieda as modified by Ohmi by using a switched capacitor circuit comprising a switch formed by connecting in parallel a p-channel MIS field-effect transistor and n-channel field-effect transistor to implement a complete switched capacitor circuit according to the teachings of Mitsuru.

20. As to claim 5, Hieda as modified by Misturu shows (Mitsuru, Fig 2) the switched capacitor circuit comprises: first p-channel and n-channel MIS field effect transistors (Mitsuru, 50,51) which receive a signal at an input terminal (1), and are connected in parallel to each other; second p-channel and n-channel MIS transistors (Mitsuru, 60,61) which are connected to each other, whose input terminals are connected to output terminals of the first p-channel and n- channel MIS field-effect transistor, and whose output terminals are grounded; a capacitor (Mitsuru, 4) one terminal of which is connected to an output terminal of the first p-channel and n-channel MIS field-effect transistors; third p-channel and n-channel MIS field-effect transistors (Mitsuru, 70,71) which are connected in parallel to each other, whose input terminal is connected to another terminal of the capacitor, and whose output terminal is grounded; and fourth p-channel and n-channel MIS field-effect transistors (Mitsuru, 80,81) which are connected in parallel to each other and whose input terminal is connected to another terminal of the capacitor.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E. Patton whose telephone number is 571-272-9762. The examiner can normally be reached on 7:00 - 5:30 Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tarifur Chowdhury can be reached on 571-272-2287. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paul E Patton
Examiner
Art Unit 2809

PEP

KIMBERLY D. NGUYEN
PRIMARY EXAMINER